

The Effects of Activation Annealing on the Reliability of Indium-Gallium-Zinc Oxide Thin-Film Transistors with Thermally Induced Source/Drain Regions

Jiapeng Li, Lei Lu, Zhuoqun Feng, Hoi Sing Kwok, Fellow, IEEE and Man Wong, Senior Member, IEEE

Department of Electronic and Computer Engineering
The Hong Kong University of Science and Technology, Clear Water Bay, Kowloon, Hong Kong

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ABSTRACT

With gas-permeable and -impermeable covers placed respectively above the channel and source/drain regions, indium-gallium-zinc oxide thin-film transistors with thermally induced homojunctions have been realized and shown to exhibit superior characteristics and small device footprint. Presently reported is the dependence of the reliability of such transistors on the heat-treatment process used for activating the homojunctions.

1. INTRODUCTION

Due to its relatively high carrier mobility, low processing temperature and transparency in the visible spectrum [1], indium-gallium-zinc oxide (IGZO), a member of the family of metal-oxide (MO) semiconductors, has been popularly investigated as a replacement of silicon in the construction of thin-film transistors (TFTs) for flat-panel displays.

Conventional back-channel-etched (BCE) or etch-stop (ES) architecture [2] is commonly adopted when making an IGZO TFT. However, the high resistance of the intrinsic MO source/drain (S/D) regions generally results in high contact resistance, hence degraded device performance. The high parasitic resistance could be reduced by increasing the conductivity of the S/D regions at the expense of increased process complexity, such as by impurity doping or plasma treatment [3] [4].

Recently, it has been reported that the resistivity of MOs capped with covers of different gas-permeability can be thermally modulated [5]. Respectively under permeable and impermeable covers, both high and low resistivity MO regions can be simultaneously realized when thermally annealed in an oxidizing atmosphere. Based on this mechanism and without increasing process complexity, an IGZO TFT with thermally induced, highly insulating channel and highly conductive S/D regions has been realized. The resulting TFT exhibits roughly the same small device footprint of a BCE TFT and the good device characteristics of an ES TFT [6], [7].

Performed in an oxidizing atmosphere at the end of the process flow, the effects of the conductivity-modulating thermal treatment on the stability of the TFT against illumination and electrical stress have been studied and are presently reported. A variety of stress conditions has

been studied, including negative/positive bias stress (N/PBS) without and with illumination (N/PBIS).

2. EXPERIMENTAL AND RESULTS

2.1 TFT Fabrication

The fabrication of an IGZO TFT with thermally induced S/D regions started with the sputtering and patterning of indium-tin oxide as the bottom-gate electrode on an oxidized silicon wafer substrate. A gate insulator of low-temperature silicon oxide (SiO_x) was then deposited. This was followed by the deposition in a radio-frequency magnetron sputtering machine of the active IGZO layer. For the Type-P TFT with the cross-section shown in Figure 1a, a bilayer of plasma-enhanced chemical vapor deposited silicon nitride (SiN_y) on SiO_x was subsequently formed. Alternatively for the Type-M TFT with the cross-section shown in Figure 1b, a single layer of SiO_x was formed.

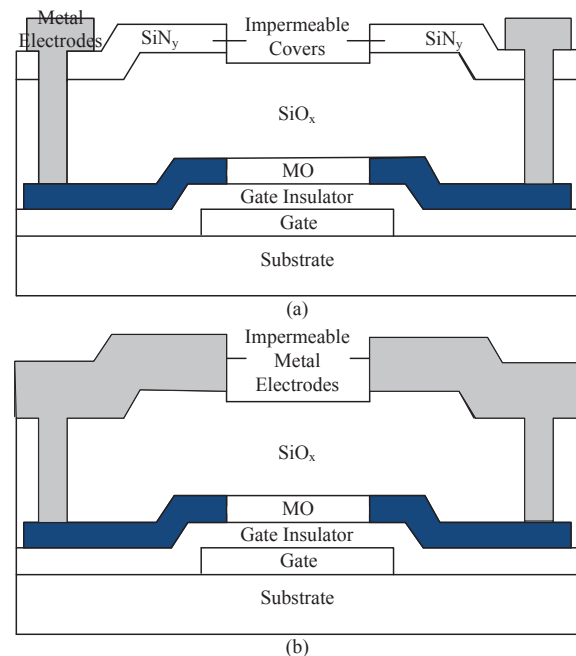


Figure 1. TFT Architectures

Schematic cross-sections of TFTs with thermally induced, highly conductive S/D regions: (a) Type-P TFT with SiN_y as the impermeable cover and (b) Type-M TFT with the metal electrodes as the impermeable covers.

For Type-P TFT, the top gas-impermeable SiN_y was removed from the channel region but retained in the S/D regions of the TFT. After the opening of the contact holes, a sputtered aluminum/molybdenum (Al/Mo) bilayer was deposited and patterned to form the metal electrodes. For Type-M TFT, the metal electrodes were extended over the channel region and used as the gas-impermeable S/D covers. The advantage of Type-M over Type-P TFT is the saving of a masking step. The S/D regions of the TFT were “activated”, i.e. turned highly conductive, during a post-metallization thermal treatment at 400 °C in oxygen (O₂) for different durations. The channel region covered with permeable SiO_x was continuously oxidized and retained its insulating property.

The electrical performance and reliability of the TFTs were characterized using an Agilent 4156C Semiconductor Parameter Analyzer.

2.2 Electrical Characteristics and Reliability

Shown in Figure 2 is the drain current (I_d) vs. gate voltage (V_g) transfer characteristics taken at a drain voltage (V_d) of 5 V of a Type-P TFT subjected to an activation anneal of 30 mins. A turn on voltage (V_{on}) of ~-1 V, a steepest subthreshold swing (SS) of ~160 mV/decade, and a peak saturation field-effect mobility (μ_{FE}) of ~5 cm²/Vs extracted from the maximum of $\partial I_d^{0.5} / \partial V_g$ were obtained. The TFT exhibits a relatively large on-off current ratio of >10⁸, due to the low off-current resulting from the strongly oxidized channel region.

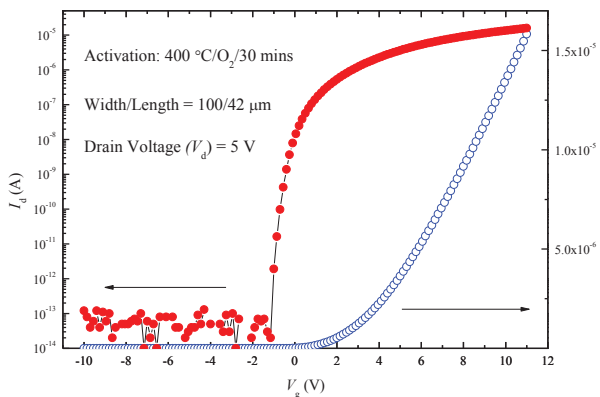


Figure 2. Transfer Characteristics

The transfer characteristics of Type-P TFT with S/D regions activated in O₂ at 400°C for 30 mins.

The stability of the Type-P TFTs subjected to P/NBS and P/NBIS, with grounded S/D regions at respective gate drive $V_g - V_{on}$ of +20 and -20 V was investigated. The illumination was performed using light with ~500 nm wavelength at a power density of 0.2 W/m². Shown in Figure 3 is the time evolution of the transfer characteristics of a TFT after NBIS. A severe negative V_{on} shift (ΔV_{on}) of over 9 V was observed, with un-degraded μ_{FE} and SS. The negative ΔV_{on} is usually attributed to the trapping of holes at the interface of the MO channel and the gate insulator. The generation of holes is related to photo- or thermal

excitation of electrons from the defect levels to the conduction band [8]–[11]. After 10,000 s of bias stress, the TFT was left in air and the transfer curves were measured after 10 and 60 mins of spontaneous recovery. It can be seen that the extent of the recovery was rather limited, reflecting a relatively long time-constant for the de-trapping of holes from the interface states.

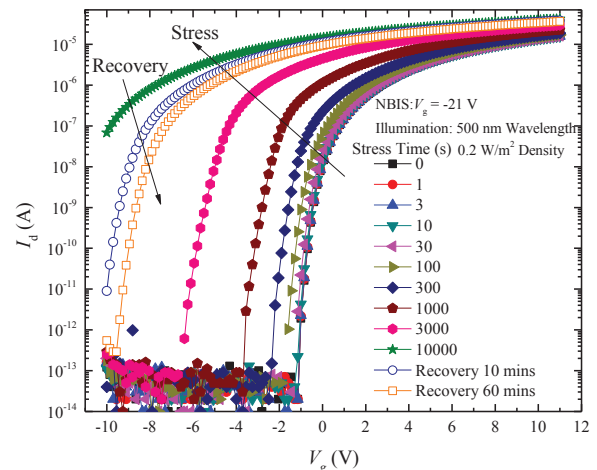


Figure 3 NBIS and Type-P TFT

The time evolution of the transfer characteristics of a Type-P TFT with S/D regions activated in O₂ at 400°C for 30 mins and subjected to NBIS.

Type-P TFTs with the S/D regions activated for different durations were fabricated. Subjected to NBS, PBS and PBIS, the dependence of the ΔV_{on} after 10,000 s bias stress of the TFTs on the activation time was measured and displayed in Figure 4.

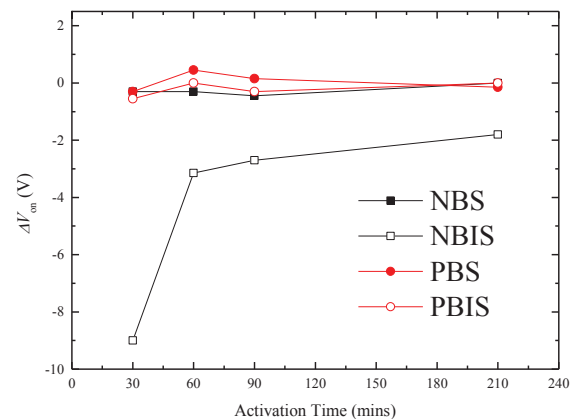


Figure 4. Reliability and Activation Time

The dependence of ΔV_{on} of Type-P TFTs on the activation annealing time.

Unlike the drastic NBIS-induced V_{on} shift, negligible change (smaller than ~0.5 V) in V_{on} was observed under these alternative stress conditions. The reliability against NBIS improved (i.e. smaller ΔV_{on}) with longer activation time. This is attributed to the continued annihilation of oxygen vacancy defects in the channel region of a TFT during an extended activation anneal. The improvement

is significant between 30 and 60 mins of activation, with diminishing return (i.e. saturation in ΔV_{on}) upon longer durations.

The reliability of Type-M TFTs has also been studied. The dependence of the NBIS-induced ΔV_{on} on the stress time is shown in Figure 5 for Type-M TFTs after 4 (a) and 6 (b) hours of activation anneal. The stress-induced shift was clearly more severe for the former than for the latter, with the former showing also a degradation in SS. Clearly, excellent stability was obtained for Type-M TFT subjected to a 6-hour activation anneal.

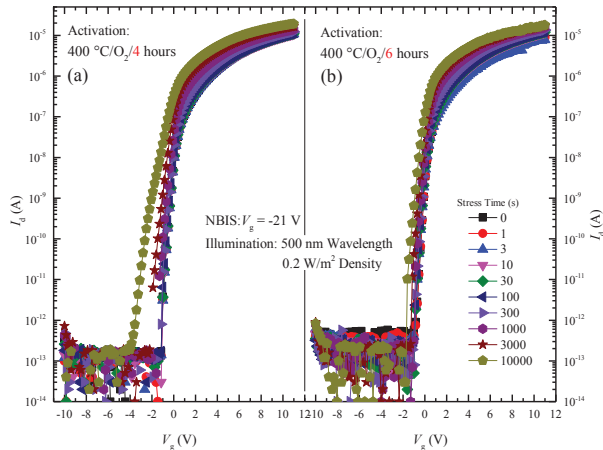


Figure 5. NBIS of Type-M TFTs

The effects of the stress time on the NBIS characteristics of Type -M TFTs subjected to 4 (a) and 6 (b) hours of activation anneal.

The reliability of Type-M TFTs activated for 6 hours and subjected to alternative stress tests was also studied and the results shown in Figure 6. In addition to the room temperature stress, N/PBS was also performed at an elevated temperature of 60 °C (commonly known as N/PBTS). The transfer characteristics hardly changed throughout the 10,000 s stress, as is evident from these characteristics. Such good stability is again consistent with the annihilation of defects in the channel region during the oxidizing activation anneal.

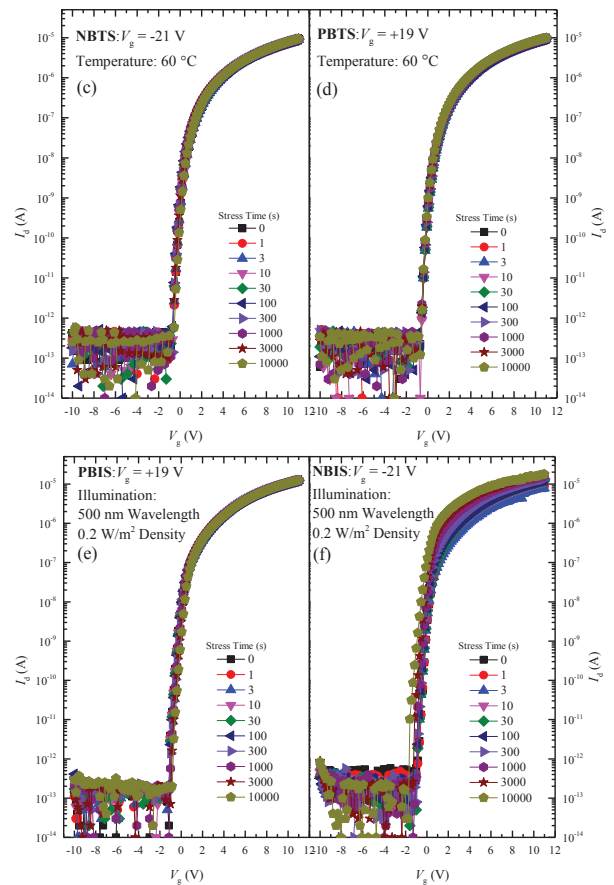
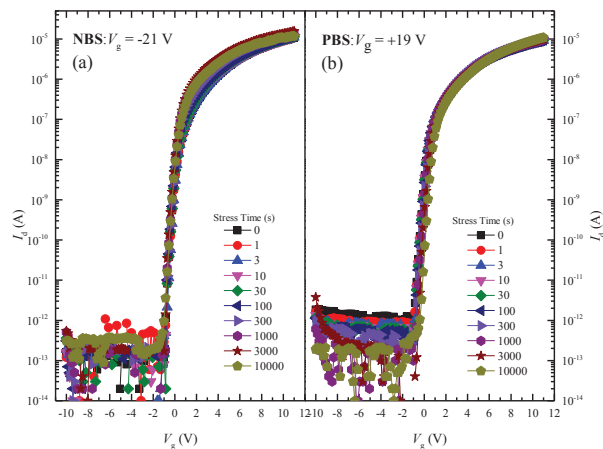


Fig. 6 Reliability of Type-M TFTs

The time evolution of the transfer characteristics of Type-M TFTs activated in O₂ at 400°C for 6 hours subjected to a variety of stress conditions .

3. CONCLUSION

Based on the mechanism of thermal modulation of the conductivity of metal-oxide semiconductors, an IGZO TFT with thermally induced, highly conductive S/D regions is proposed and demonstrated. The resulting TFT is found to exhibit both good device characteristics and small footprint. The dependence of the reliability of the TFT against a variety of stress conditions was thoroughly studied. It is found that with a sufficiently long activation anneal in an oxidizing atmosphere, good reliability can be obtained. This improvement is attributed to the annihilation of oxygen vacancy defects in the channel region of the TFT.

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